A *Ka*-BAND PLANAR TRIPLER BASED ON A STACKED SYMMETRIC InP HETEROSTRUCTURE-BARRIER VARACTOR

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ABSTRACT

The symmetric heterostructure barrier varactor (HBV) lends itself to frequency tripling with no need for bias or for a second harmonic idler circuit. This paper presents the performance of the first planar microstrip *Ka*-band frequency tripler based on a *stacked* HBV structure. A minimum conversion loss of 11.2 dB with a maximum power output of 10.78 dBm at 40.35 GHz is obtained.

INTRODUCTION

The symmetric HBV (also known as the single-barrier varactor or quantum-barrier varactor) has a symmetric $C(v)$ and an antisymmetric $i(v)$ characteristic, both centered around zero bias. Waveguide triplers without idlers or bias circuits have been demonstrated previously using symmetric HBVs, but the output power levels reported have been very low (less than 1 mW), and efficiencies have been poor [1,2,3]. Moreover, because of excessive leakage currents, output power saturation has occurred at low input-power levels.

By stacking three varactor layers [4] we find that it is possible to fabricate symmetric HBV devices that are characterized by:

- Very low leakage,
- Low capacitance per unit area, and
- High breakdown voltage.

In each of these categories, the performance exceeds that of previously-described HBVs. In addition, by using pseudomorphic InAlAs/AlAs/InAlAs barriers, we achieve excellent current blocking. Simulations indicate power outputs of 50 mW at 39 GHz, 40 mW at 90 GHz, and 20 mW at 186 GHz [4].

We have employed this stacked device in a 5-mil alumina circuit to realize a planar symmetric-HBV tripler that requires neither idler nor bias circuits. This tripler circuit is free from the output-power saturation problems caused by undesired resistive nonlinearities, that have been reported by previous authors [1,2,3].

THE DEVICE

An HBV consists of a thin barrier-layer of large-bandgap material, on either side of which is a thick layer of smaller-bandgap material. We stack three iterations of these barrier and depletion layers to obtain a symmetric varactor whose $C(0)_{stacked}$ is $C(0)_{single}/3$. The layers of this stacked device are shown in Figure 1; details of the growth and processing can be found elswhere [4].

The device was characterized by making accurate small-signal measurements of its impedance at various bias points. The low-leakage characteristics of the stacked varactor are evident from the $\Re e\{Z_{11}\}$ measurements shown in Figure 2. The breakdown voltage is approximately 14.25

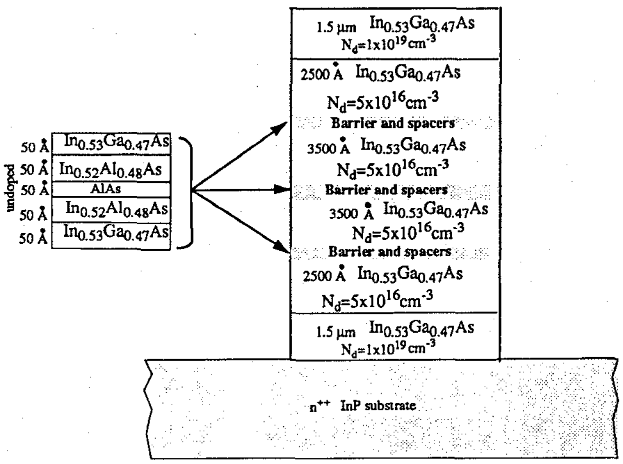

Figure 1. MBE layers of the stacked InP varactor.

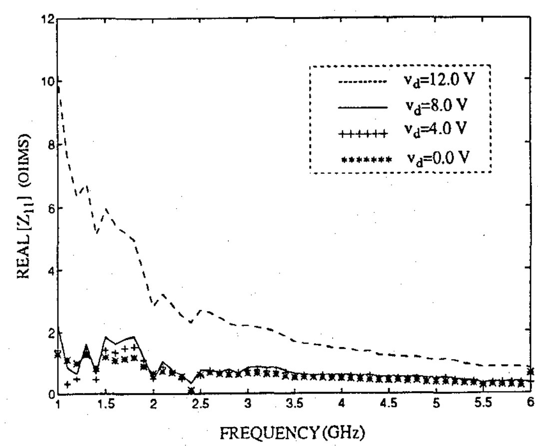

Figure 2. Low-leakage characteristics of a 36 μm-diameter stacked varactor on InP.

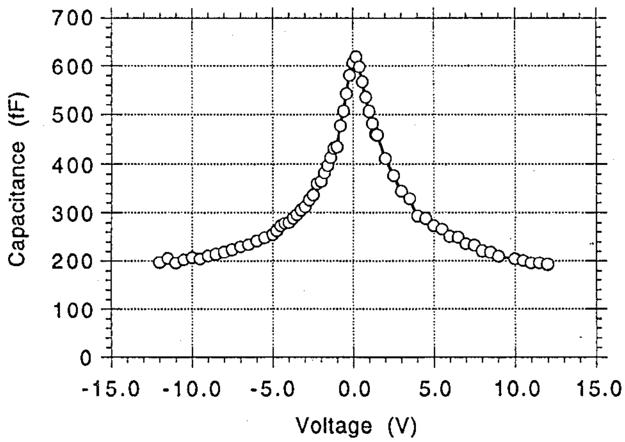

Figure 3. $C(v)$ characteristic of a 36 μm-diameter stacked varactor on InP.

V, compared with 5.7 V for a single-barrier non-stacked device. A 36-μm diameter device yields a $C(0)$ of 0.6 pF, a C_{max}/C_{min} ratio of 3 and an R_S of 0.37 Ω, with a cutoff frequency of 1.434 THz. The measured $C(v)$ curve is shown in Figure 3.

PLANAR TRIPLER

Figure 4 shows a photomicrograph of the planar tripler as realized using 5-mil alumina input and output substrates. The device chip is shunt-mounted on a grounded heat sink. The top of the mesa is ribbon-bonded to the input and output circuits. At the input there is a low-pass filter and a matching circuit to the device; the output matching circuit is followed by a coupled-line bandpass filter. The circuit is so designed that the input is isolated from the output and *vice versa*.

The circuit design begins by determining the equivalent large-signal pumped impedances at the plane of the device at both the fundamental and third-harmonic frequencies. This can be done either by using Seigel and Kerr's method [5], or by means of the empirical "cubic $v(q)$" model [6]. The procedure continues by designing input and output circuits that match the equivalent device impedances at the corresponding frequencies to the 50-Ω external environment. The input matching transformer [7], see Figure 5, consists of a λ/4 low-impedance section followed by a high-impedance λ/8 section. For design purposes, the bond ribbons are modelled as distributed air-dielectric transmission lines at an average height above a ground plane [8]. The input low-pass filter is a sequence of high-impedance/low-impedance sections, while the output

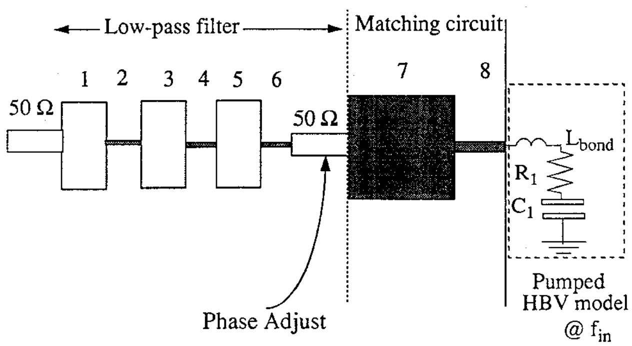

Figure 5. Input circuit of the planar 13-to-39 GHz tripler. LPF dimensions (τ = mil): $W_1 = W_3 = W_5 = 26.5$ τ, $L_1 = 13$ τ, $L_3 = 15$ τ, $L_5 = 10.2$ τ, $W_2 = W_4 = 1.9$ τ, $L_2 = 47.1$ τ, $L_4 = 86.5$ τ, $L_6 = 35$ τ. Matching circuit dimensions: $W_7 = 53.5$τ, $L_7 = 73$ τ, $W_8 = 7$ τ, $L_8 = 31$ τ.

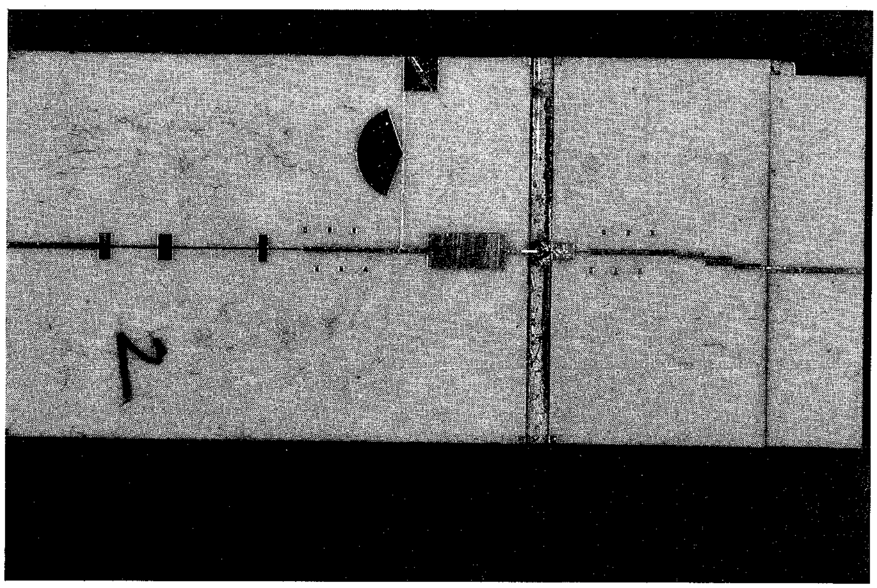

Figure 4. Photomicrograph of the planar Ka-band tripler.

bandpass filter, see Figure 6, is a coupled microstripline structure. The design is completed by including 50-Ω phase-adjust lines in between the matching networks and the filters. These phase-adjust lines serve to "move" the filter positions electrically, so that at the device plane, the input filter presents an open circuit to the third harmonic, while the output filter presents an open circuit to the fundamental.

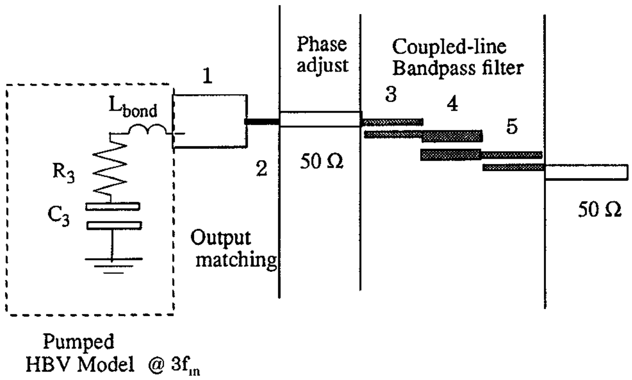

Figure 6. Output circuit of the planar 13-to-39 GHz tripler. Matching circuit dimensions (τ = mil): W_1 = 16 τ, L_1 = 22.3 τ, W_2 = 1.6 τ, L_2 = 15.2 τ. BPF dimensions: $W_3 = W_5$ = 2.43 τ, $L_3 = L_5$ = 28.9 τ, $S_3 = S_5$ = 1.0 τ, W_4 = 3.6 τ, L_4 = 28.0 τ, S_4 = 2.0 τ.

EXPERIMENTAL RESULTS

As indicated in Figure 7, the input signal to the tripler is derived from an HP 8350B sweep oscillator, with an HP 8344 solid-state power amplifier to increase the power level to a maximum of ~24 dBm. A harmonic-reject filter is used to remove the second and third harmonics that can be produced when the amplifier goes into saturation. The actual input power to the tripler is monitored by means of an HP 8485 power detector and an HP 438A power meter, and has to be corrected for cabling and filter losses.

The tripler is mounted in the jaws of a Wiltron Universal test jig type 3680K. The output is extracted via a K-connector cable followed by a coaxial-to-WR-28 adaptor, a coupler and an HP 8486A power detector. An isolator is used to counter the effects of the non-ideal loading of the power detector. The WR-28 waveguide has a passband from 26-40 GHz. The input to the tripler is fixed at either 18 dBm or 22 dBm.

The input power to the tripler was set to either 18 dBm or 22 dBm. With the 22-dBm input the tripler was found to saturate. This input level also represents the maximum power obtainable from the power amplifier at 13.0 GHz. To compensate for input-power variations incurred in sweeping the input frequency from 13.0 to 14.0 GHz, the power level was adjusted to maintain a constant input drive level to the tripler.

Figure 8 shows the measured power output P_{out} at the tripled frequency for both the 18-dBm and 22-dBm input levels P_{in} in the range 13.0 to 14.0 GHz. The relatively narrow bandwidth of the response is due to the low impedances that have to be matched to 50 Ω. These

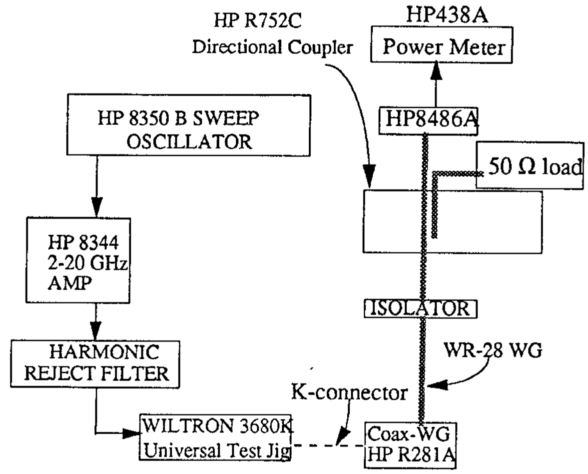

Figure 7. Experimental setup used to measure tripler performance.

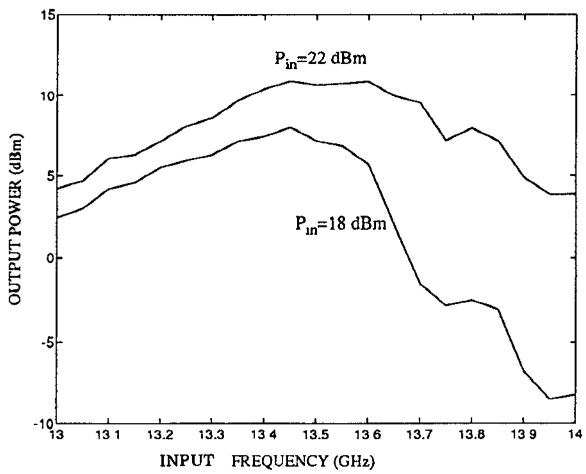

Figure 8. Frequency response of the tripler, shown at P_{in} = 18 dBm and at P_{in} = 22 dBm.

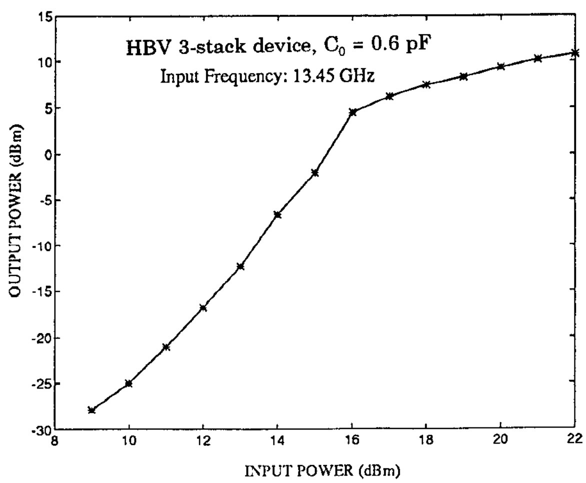

Figure 9 The tripler P_{in} versus P_{out} transfer function at the center input frequency 13.45 GHz. The output frequency is 40.35 GHz.

impedances are a consequence of the high zero-bias capacitance (0.6 pF) of the HBV. The bandwidth could be improved by reducing the device area.

Figure 9 depicts the P_{in} versus P_{out} characteristics of the tripler at the center frequency of 13.45 GHz. A minimum conversion loss of 11.22 dB with a maximum power output of 10.78 dBm is obtained at 40.35 GHz.

DISCUSSION

This experiment demonstrates the first planar tripler to use stacked HBVs. The output of 10.78 dBm is smaller than the theoretically-predicted 17 dBm, but is sufficient to drive a double-balanced mixer. The output power P_{out} is limited by the availability of source power. An experimental *waveguide* tripler tested at Philips Microwave (Hazel Grove, U.K.) has yielded a maximum power output of 20 dBm with 7-dB conversion loss using the same device [9]. The second harmonic was found to be well rejected by the device/circuit combination, with a value of -38 dBc with respect to the third harmonic. The input signal power leakage at the output was -16 dBm for a P_{in} of 18 dBm. This planar tripler performance is comparable with that of an idler-based *Ka*-band classical varactor tripler reported earlier [10].

ACKNOWLEDGEMENTS

We acknowledge the assistance of Mr. Gary Smith, Mr. John Ovey and Dr. Chris Rogers at Philips Microwave, Hazel Grove, Stockport, Cheshire, UK; the help and hospitality of Professor Erik Kollberg at the Chalmers University of Technology, Gothenburg, Sweden; and the financial support of the Defence Research Agency, Malvern, UK, and of the Natural Sciences and Engineering Research Council of Canada .

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